

# MLCA\_4

Oct 19, 2000



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<b>AllianceCORE™ Facts</b>	
<b>Core Specifics</b>	
Supported Family	SPARTAN
Device Tested	XCS30-4 (VQ100 case)
CLBs <sup>1</sup>	443
Clock IOBs <sup>2</sup>	1
IOBs	63
Performance (MHz)	33
Xilinx Core Tools	M1.5i
Special Features	Logiblox 32 bit counter
<b>Provided with Core</b>	
Documentation	User guide, design guide
Design File Formats	EDIF netlist
Constraints Files	Filename.ucf
Verification	VHDL Model, Test bench
Instantiation templates	VHDL, ( <i>Verilog, Viewlogic symbol</i> )
Reference designs & application notes	None
Additional Items	None
<b>Simulation Tool Used</b>	
Aldec ActiveVHDL	
<b>Support</b>	
Support provided by MEET Ltd	

Notes:

1. Utilization numbers for Virtex are in CLB slices
2. Assuming all core I/Os are routed off-chip

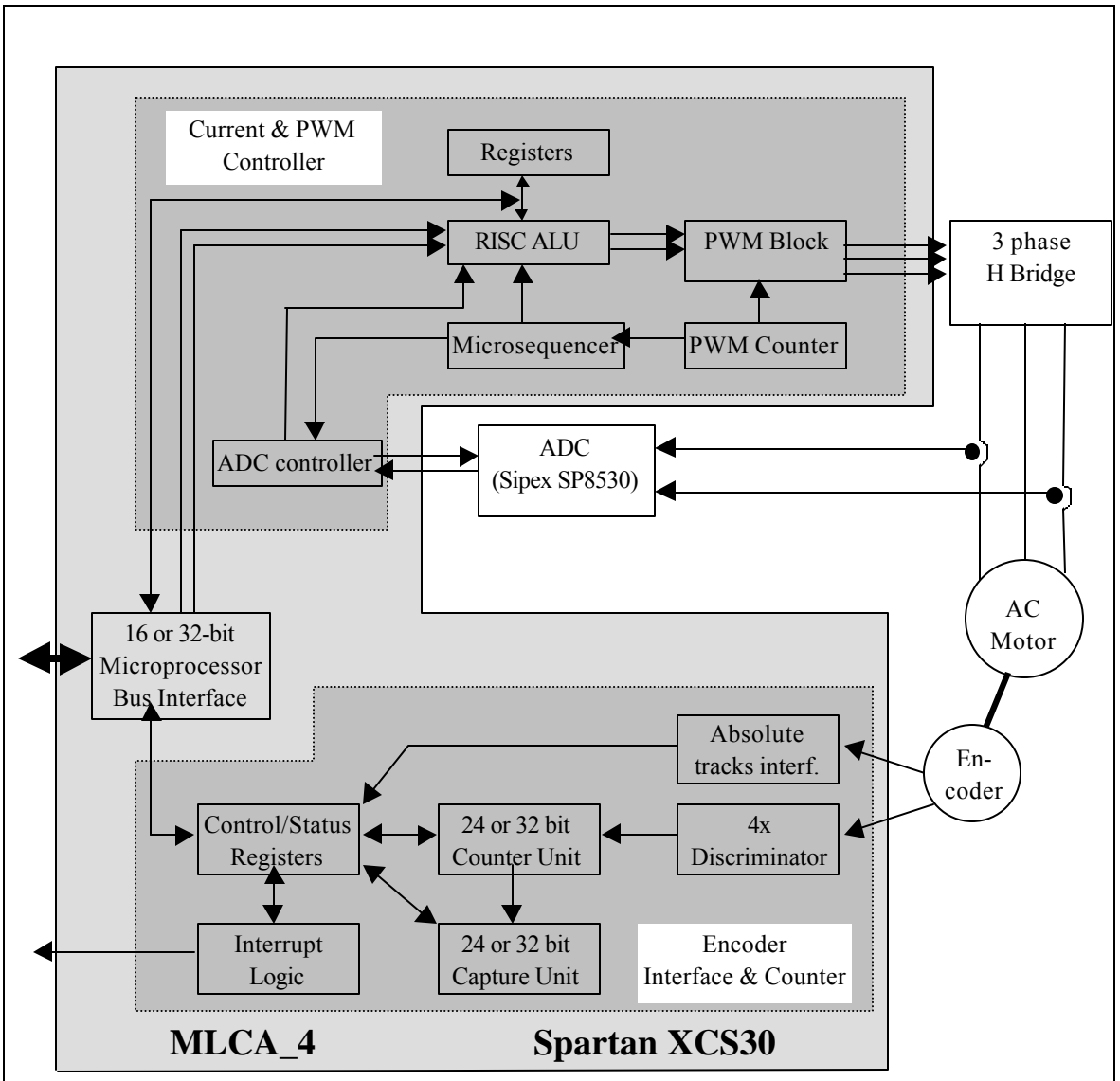


Figure 1: MLCA\_4 Block Diagram

## Features

- fast configurable 16 or 32 bit microprocessor bus interface
- programmable digital P or PI-type current regulator
- current regulation cycle time of 62 usec (@33MHz clock)
- integrated 3-phase PWM generator
- symmetrical PWM waveform with programmable dead time
- glueless interface to external current sensing ADC
- optical encoder interface with 32 bit counter/capture unit and various error detection mechanisms
- 14 easy to learn memory mapped registers
- small 100 pin TQFP package

## Applications

- Robotics
- Industrial controls
- High speed servo positioning systems

- current controlled power supplies/inverters

## General Description

The core contains all the peripheral circuitry usually found in processor based servo drives. It offers a complete 3 phase servo motor current control system, a 3 phase PWM generator and an optical encoder interface with discriminator and counter in one package. It acts as a coprocessor to a microcontroller, offloading everything except the position control algorithm.

## Functional Description

The current controller is based on a 10 bit RISC ALU that executes a 3 phase P or PI control algorithm in microcode. The control parameters are programmable. The current feedback information is obtained through an external ADC (Sipex SP8530) that is directly controlled by the core over a glueless interface.

The PWM unit generates symmetrical, center-aligned waveforms to drive 6 power transistors. The dead time to avoid vertical "shoot-thru" is programmable.

The encoder interface provides a "4x" discriminator and a preloadable 32 bit position counter. Other features such as a capture function (with its own 32 bit counter image register), counter auto-zero (for rotating axes) and a full range of error detection mechanisms are included as well.

## Core Modifications

None at this moment.

However, a reduced size version with a 16 or 24 bit optical encoder counter-capture unit (instead of 32 bit) and/or a fixed-width 16 bit external data bus could be delivered shortly.

Upon request, it is possible to have only either the optical encoder or the current controller subunit.

Future additions reserved.

## Pinout

Signal	Signal Direction	Description
<b>Microprocessor bus interface</b>		
ADDR (3-0)	Input	Address bus 3-0
XDATA (15-0)	In/Out	Data bus 15-0
XDATA (31-16)	In/Out/Z	Data bus 31-16 <i>(optional)</i>
/CS	Input	Chip select
/RD	Input	Read
/WR	Input	Write
/INT	Output	Interrupt <i>(optional)</i>
<b>Clock, Reset, Mode</b>		
CLK	Input	Master clock
/MRES	Input	Master reset
DHE	Input	Ext. Data bus size

<b>Optical Encoder Interface</b>		
Enco_A	Input	Incremental track 'A'
Enco_B	Input	Incremental track 'B'
Enco_Z	Input	Reference mark ('Zero')
Enco_U	Input	Absolute track 'U' <i>(optional)</i>
Enco_V	Input	Absolute track 'V' <i>(optional)</i>
Enco_W	Input	Absolute track 'W' <i>(optional)</i>
Ext_Latch	Input	Capture event trigger input
Error	Output	Quadrature discrim. error
Aux_in	Input	Auxiliary input flag
<b>Current controller &amp; PWM section</b>		
PWM1	Output	High side drive, phase 1
PWM2	Output	High side drive, phase 2
PWM3	Output	High side drive, phase 3
NPWM1	Output	Low side drive, phase 1
NPWM2	Output	Low side drive, phase 2
NPWM3	Output	Low side drive, phase 3
PWM_STOP	Input	Shutdown of all PWM outputs ("safety off")
<b>ADC Interface (motor current sense) (for Sipex SP8530)</b>		
AD_CLK	Output	ADC serial clock
AD_CS	Output	ADC chip select
AD_IN	Input	ADC serial data
AD_STAT	Input	ADC status flag

## Critical Signal Descriptions

The most critical part is the 32 bit encoder counter. For this reason, this block is built using a Xilinx Logiblox.

## Core Assumptions (Optional)

none

## Verification Methods

VHDL simulation model with SDF timing file.

## Recommended Design Experience

Required experience:

- 3 phase PWM current control power circuits (including power drivers and isolated current measure)
- microprocessor peripheral interfacing (Intel style bus).
- Xilinx FPGAs and development tools

## Ordering Information

Contact

- MEET Ltd, or
- Xilinx Inc.

## Related Information

### Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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